L- AND S- BAND 50-WATT POWER GaAs MESFETs

Hiroshi Ishimura, Masaya Murayama, Kazuhiro Arai,
Yasunobu Saito, Yuji Oda and Hiromichi Kuroda

Microwave Solid-State Department
Komukai Works
Toshiba Corporation
1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan

Abstract

L- and S-band high power GaAs FETs have been developed. At 1.8 GHz, the FET delivers an output power at 1 dB gain-compression point of 42.7W (46.3 dBm) with 13.3 dB gain and 42 % power-added efficiency, and a saturated output power of 51.3W (47.1 dBm). The developed FETs will contribute to improve the performance of microwave SSPAs used in various radar and communication systems which require higher output power and low distortion.

1. Introduction

The usage of solid-state devices is the key to achieve long-term reliability of microwave communication and radar systems. High power GaAs FETs have been widely used in the solid-state amplifiers (SSPAs) replacing the travelingwave tubes (TWTs) in accordance with the improvements of the FET power performances. Market demands for high power FETs, therefore, are still increasing.

In this paper, power performances of newly developed L- and S-band GaAs MESFETs are reported. The characteristic feature is that the FETs are fabricated by using the ion implantation technology which is favorable in terms of uniformity, reproducibility, flexibility of device processing, and thus, low cost fabrication. Some improved gate structures for GaAs MESFETs have been proposed to improve the breakdown voltage and thus the power handling capability of the single FET chip[1]. In this study, a double recessed gate structure is introduced in order to reduce the source resistance with keeping the drain breakdown voltage at a high enough level and ion implant conditions are optimized for the structure. The FETs deliver an output power at 1 dB gain-compression point of 42.7W (46.3 dBm) with 13.3 dB gain and 42 % power-added efficiency, and a saturated output power of 51.3W (47.1 dBm) at 1.8 GHz. These output powers are the highest values reported so far on power GaAs FETs.

2. Fabrication Process and Chip Design

A schematic cross section of the fabricated FET is shown in Figure 1. At first, n^+ layers for source and drain are implanted with a dose of 2.0×10^{13} Si/ cm^2 successively at 50 keV, 120 keV and 250 keV. Then, an n-type channel layer is formed by selective implantation at 150 keV with a dose of 3.8×10^{12} Si/cm^2 . The implanted wafers are capless-annealed at 850 °C for 15 minutes[2]. The peak carrier concentration of the channel layer is about 1.6×10^{17} cm^{-3} .

The keys to improve power handling capability of the single FET chip and to achieve higher output power are reducing the source resistance and increasing the both gate and drain breakdown voltages. A double recessed structure as shown in Figure 1 is introduced to obtain lower source resistance and higher drain breakdown voltages.

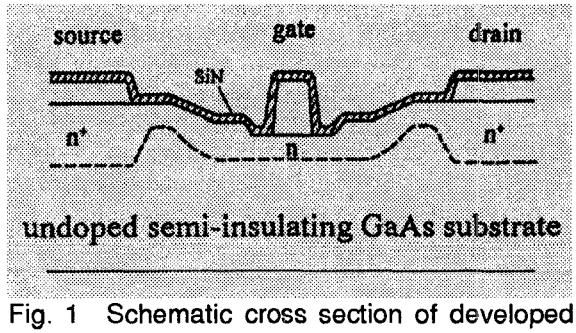

Fig. 1 Schematic cross section of developed FET chip.

0-7803-3246-6/96/$5.00 © IEEE

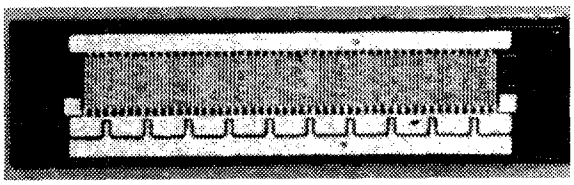

Fig. 2 Top view of FET chip. (total gate width = 26 mm, chip size = 3.0 mm x 0.8 mm)

The double recessed structure is also favorable to increase the output drain resistance, and this leads to higher gain. The channel doping profile, which is controlled by implanted ion species, energy and dose, is optimized for the structure taking the aspect ratio (gate length/ channel thickness) into account.

The source and drain ohmic contacts are formed by alloying Pt/AuGe. The Ti/Al gate is delineated by i-line lithography and passivated with SiN film.

The air-bridge crossover structures are used to reduce parasitic capacitance. The GaAs wafer is thinned to 40 μm . A gold plated heat sink (PHS) technology and source via-hole connection to the back side PHS are adopted to reduce thermal resistance and to minimize the source grounding inductance.

Figure 2 shows the top view of the FET chip. The FET chip has been designed to highly integrate the active region. The gate length and the unit gate finger width of the chip are 1.0 μm and 260 μm, respectively. Total gate width is 26 mm and the chip size is 3.0 x 0.8 mm.

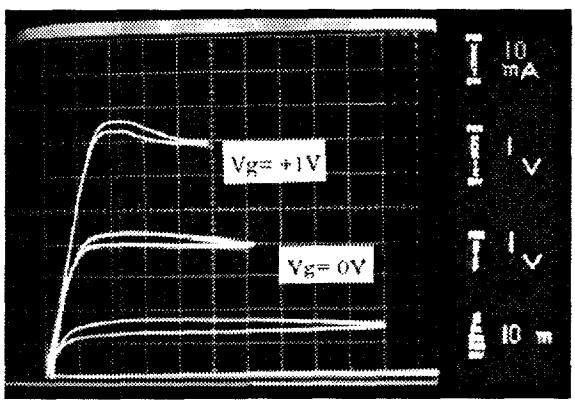

Fig. 3 I-V characteristics of the unit FET (Wg = 260 μm)

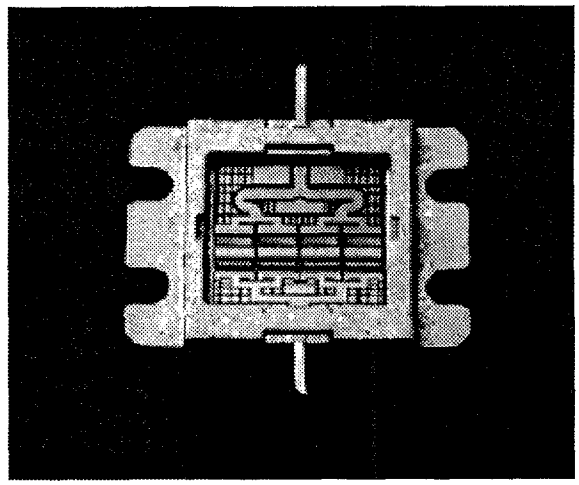

Fig. 4 Internal view of 4-chip FET. (total gate width = 104 mm)

3. FET Performance

Figure 3 shows the I-V characteristics measured for a unit FET (1-finger FET, Wg=260 μm) in the TEG(Test Element Group) which is fabricated simultaneously on the same wafer. Clear pinch-off characteristics and small drain conductance have been obtained as shown in Fig. 3. The ratio of the maximum drain current(Idsmax) to the saturated drain current(Idss) of the FET is estimated around 1.7. This high enough Idsmax together with the high drain breakdown voltage leads to high output power density.

Four-chip devices are assembled in metal-wall packages for DC and RF(microwave) measurements. The 4-chip FET is assembled with impedance transforming circuits using lumped and distributed elements. The power combining circuit transforms the output impedance of the 4-chip FET to around 20 Ω. Figure 4 shows the internal view of the 4-chip FET which has a total gate width of 104 mm.

Typical Idss, transconductance, and pinch-off voltage are 16 A, 6.2 S, and 2.0 V, respectively, for the 4-chip FET. The drain breakdown voltage is more than 20 V at a current level of 1 mA / mm.

A typical thermal resistance has been estimated to be about 1 °C/W by IR measurements.

The rf performance of the 4-chip FET at 1.8 GHz under a drain voltage of 10 V are shown in Figure 5. The FET delivers an output power at 1 dB gain-compression point of 42.7W (46.3 dBm) with 13.3 dB gain and 42 % power-added efficiency, and

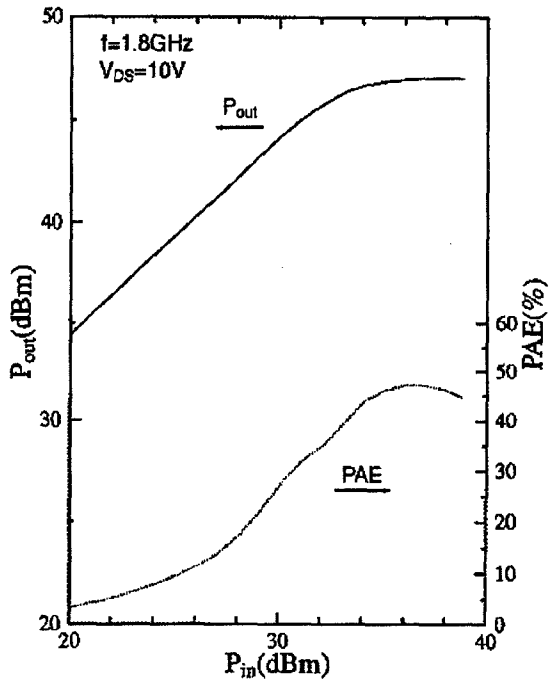

Fig. 5 Output power and power-added efficiency versus input power at 1.8 GHz of developed FET.

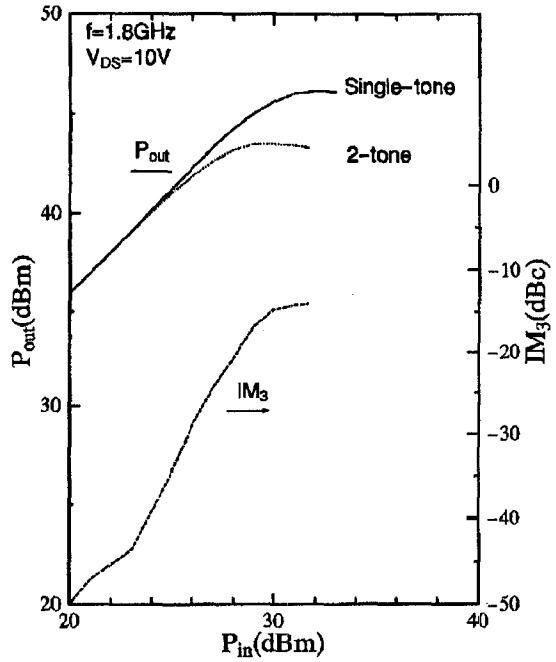

Fig. 6 Third order intermodulation distortion characteristics of developed FET.

a saturated output power of 51.3W (47.1 dBm) at 1.8 GHz. The FET can cover a frequency range of 1.6 - 2.0 GHz with a gain flatness of ± 0.5 dB. By selecting the lumped element of the internal matching circuits, an operating frequency of the 4-chip FETs can be tuned up to an S-band. As mentioned previously, the output impedance of the FET is not fully transformed to the 50 Ω. The FET can, therefore, be tuned by external matching circuits, as well. The power performances have been found to be little degraded up to 2.6 GHz. These output powers are the highest values reported so far on power GaAs FETs.

Figure 6 shows the third order intermodulation distortion characteristics of the 4-chip FET at 1.8 GHz under a two-tone test with a frequency separation of 5 MHz. A third order intermodulation distortion of typically -45 dBc has been obtained at an output power level of 38 dBm under a two-tone test. An intercept point of more than +56 dBm has been obtained.

4. Conclusion

L- and S-band high power GaAs FETs have been developed. At 1.8 GHz, an output power of 42.7 W at 1 dB gain-compression point has been obtained with 13.3 dB gain and 42 % power-added efficiency. The FET delivers more than 50 W saturated output power from L- to S- band. Moreover, it shows an excellent linearity. The developed FETs will contribute to improve the performance of microwave SSPAs used in various radar and communication system applications which require higher output power and low distortion such as the direct satellite-based digital mobile communication systems.

Acknowledgments

The authors would like to thank K. Kamei, M. Higashiura, Y. Yamada and Dr. H. Tokuda for helpful discussions and encouragement. They also wish to acknowledge T. Asano, H. Okuda and K. Kai for their contributions to this work.

References

[1] T. Takahashi, K. Asano, K. Matunaga, N. Iwata, A. Mochizuki and H. Hirayama ; "STEP-RECESSED GATE GaAs FETs WITH AN UNDOPED SURFACE LAYER," IEDM Tech. Digest, pp.259-262, 1991.

[2] H. Ishimura, T. Udagawa, H. Kamo and M. Higashiura ; "Electrical uniformities in Si^+ implanted semi-insulating Cr-doped GaAs," Inst. Phys. Conf. Ser. No 63, pp. 377-382, 1982.